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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,054	06/06/2001	Gary McCormack	45386/DMC/V165	1976

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CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
ZIMMERMAN, BRIAN A	

ART UNIT	PAPER NUMBER
2635	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,054	MCCORMACK ET AL.	
	Examiner	Art Unit	
	Brian A Zimmerman	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26,30-33,35-37,39,40,42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26,30-33,35-37,39,40,42 and 43* is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

EXAMINER'S RESPONSE

Status of Application

In response to the applicant's amendment received on 6/18/04. The examiner has considered the new presentation of claims and applicant arguments in view of the disclosure and the present state of the prior art. And it is the examiner's position that claims 1-25 are unpatentable for the reasons set forth in this office action:

This case has been reassigned to a new examiner. Accordingly, all correspondence regarding this case should reflect the new examiner.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-4,13-15,23 rejected under 35 U.S.C. 103(a) as being unpatentable over Pierro (5446424) and Dayton (5818349).

Dayton teaches of a cross point switch unit (Fig 3) comprising a switch matrix module (Fig 2) with the switch matrix module comprising active elements (24, 28, 32, 34, 40a-d), transmission lines in one direction (20), and orthogonal transmission lines in a second direction (30). Dayton teaches of programmable registers (44) coupled to the active elements (40a-d), with the active elements coupled to one transmission line in one direction and on transmission line in the other direction. It is understood in the art

that switch modules must have a programmable means to adjust the crosspoint connections through active elements. Dayton teaches of connecting a second switch matrix module (Fig 2) to the first matrix module with the output of the first matrix module connected to the input of the second matrix module (Fig 4). Dayton teaches that a programming interface (70) can be connected to the switch core (78), and that output drive levels of the output of the switch matrix (40a-d) as commanded by the programming interface (70). Dayton teaches that a programming interface (70) can be connected to the switch core (68) with output drive registers (44) coupled to the switch core, and that the switch core controls the output levels of the outputs (Fig 3). Dayton teaches of a crosspoint matrix with input lines (20) and output lines (30) coupled at certain points (40a-d) according to the shift register (78). It is understood that there is an insulating layer between input and output lines or the lines would come in contact with each other and incorrect operation of the crosspoint switch would result. Dayton fails to expressly teach the physical arrangement of the layers claimed.

In an analogous art, Pierro shows a first conducting layer having multiple transmission lines 66 and a second conducting layer having multiple transmission lines 54 with an insulating layer 56 separating the two conducting layers. The layout of the switch in Pierro includes connection tap, namely the via holes 76. See col. 10 lines 5+. On col. 10, Pierro gives various reasons why the via holes are used to make the connections between the two transmission line traces. Therefore, it would have been obvious to one or ordinary skill in the art at the time of the invention to have used the physical layout including the via holes of Pierro in the Dayton switch since such would

provide additionally functions such as serving to minimize cross coupling and interference between transmission lines.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pierro and Dayton in view of Heo et al (heretofore Heo). Dayton and Pierro, as discussed above, teach claims 1-4. The Dayton-Pierro combination does not teach of the inputs or outputs connected to the pads of a printed circuit board via a ball grid array (BGA). In an analogous art, Heo teaches the use of a semiconductor package and assembly method. Prior art figure Fig 1B shows the connection of an IC to a substrate that connects through a BGA.

It would have been obvious to one skilled in the art at the time of invention to use the switch modules of Dayton-Pierro in the prior art construction of Heo (Fig 1B) because Heo suggests that fabricating a semiconductor package in such a manner provides IC's that are light, thin, simple, and have a compact structure thereby providing an improvement in the integration degree and performance of the IC package (Col 1, lines 10-22).

3. Claims 7-12, 24,25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton and Pierro in view of Morgan et al (heretofore Morgan).

The Dayton-Pierro combination does not teach the use of a passive network coupled to the transmission lines. Morgan suggests the use of a low voltage amplification circuit that includes a passive network (16) connected to input lines (18,

21). Morgan suggests that the passive network (16) include capacitors (36, 43) and resistors (33, 41) tuned to condition the signal for the respective voltages of a low voltage differential signal applied to the terminals (Col 3, lines 56-59). Moran suggests that the passive network includes a resistor (33 or 41) and capacitor (36 or 43) in parallel (Fig 1, 23) on each of the lines of a differential signal. Placement of the Morgan's passive compensation network (16) on or off the die of the integrated circuit would have been within the scope of Morgan's invention because he describes the entire amplification circuit being implemented in an IC (Col 3, lines 7-9) and also provides that connection of any element, such as the passive compensation network (16), with other elements through direct connection on the same IC (Col 9, lines 37-41). Morgan suggests that input circuit (16) is for conditioning high-speed data signals (Col 3, lines 9-12) and as such would inherently provide decreased signal attenuation at higher frequencies. Morgan suggests the use of a differential signal path as shown by the differential signal applied to the terminals (Col 3, lines 58-59). Morgan shows that the differential signal path includes a first (18) and second (21) transmission line with the passive network (23) comprising a resistance and a capacitance with a shunt resistor connecting first and second transmission lines. Morgan does not suggest the use of multiple resistors or capacitors in series. It would have been obvious to one skilled in the art at the time of invention to place as many resistors or capacitors in series as would be necessary to achieve the desired resistance or capacitance of the compensation filter because choice of capacitance and resistance is a design choice.

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton with the suggestions of Morgan because Dayton teaches of a crosspoint switch for high-speed switching of data and Morgan teaches of an amplification circuit for use with high-speed data. In addition, Morgan suggests that such amplification circuits have such use in high-speed data transmission receivers (Col 3, lines 9-12).

4. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton, Pierro in view of Shankar et al. (heretofore Shankar).

Neither Dayton nor Pierro teaches of user of registers coupled to the switch matrix module (Fig 2) for storing programming data provided by the programming interface (70). It is known in the art that all switches usually have some type of permanent storage to store programming in order to operate such as ROM, EPROM, EEPROM, or NVRAM. Shankar suggests the use of a programmable IC switch in which user registers (250) are provided for storing programming data provided by micro-controller (220). Such programming data is used for mapping information for setting the interconnections of inputs and outputs of the switch (120).

In reference to claim 17, Dayton does not teach of staging registers connected to switch matrix module (Fig 2), and for using programming interface to store programming data previously stored in the staging registers and providing it at a later time. Shankar suggests programming switch (120) through the micro-controller (220). It is well known that micro-controllers have output registers. Shankar suggests using output registers

for programming switch and for storing data in user registers (250) for recalling later (Col 4, lines 54-57).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton-Pierro with the suggestions of Shankar because Dayton teaches of a switch core and Shankar teaches of how to control a switch, and Shankar suggest that his programmable IC for manipulating a switch provides a simple and versatile programming process (Col 1, lines 45-54).

5. Claims 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton, Pierro in view of Murata et al. (heretofore Murata).

In reference to claims 18,21 Dayton-Pierro does not teach that the programming interface is configured to provide programming data that associates consecutive outputs to inputs as specified by the programming interface. In an analogous art, Murata teaches of a programming interface (4) that provides programming data (S2) to a switch configuration management unit (5) that logically associates consecutive outputs to inputs as specified by programming interface (4).

In reference to claims 19,22 Dayton-Pierro do not teach that programming interface is configured to group inputs and outputs of the switch matrix module. Murata teaches that programming interface provides programming data to management unit that logically groups inputs and outputs.

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton-Pierro with the suggestions of Murata because Dayton

remains silent about a programming interface, and Murata suggests a programming interface that uses a virtual control for associating input and output terminals. An artisan skilled in the art at the time of invention would have been motivated to combine the teachings of Dayton with the suggestions of Murata because Murata's virtual control provides more efficient use of input and output ports (Col 1, lines 36-43). In addition, Murata discloses that prior art switchers input and output lines are arranged in the form of a matrix so that it is possible to switch the output destinations of the input signals or simultaneously distribute the input signals to a plurality of output lines in accordance with a user's instruction (Col 1, lines 16-21).

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dayton, Pierro and Shankar in view of Murata.

In reference to claim 20, Dayton-Pierro-Shankar does not teach that programming interface can associate the groups of inputs to the groups of outputs. Murata teaches that groups of inputs can be logically associated with groups of outputs (Fig 10A, 10B).

It would have been obvious to one skilled in the art at the time of invention to combine the teachings of Dayton-Pierro-Shankar with the suggestions of Murata because Dayton remains silent about a programming interface, Shankar provides the means for programming a switch such as the one disclosed by Dayton such as a micro-controller (220) and a PLD (250), and Murata suggests the use of a virtual control for associating input and output terminals. An artisan skilled in the art at the time of

invention would have been motivated to combine the teachings of Dayton-Pierro-Shankar with the suggestions of Murata because Murata's virtual control provides more efficient use of input and output ports (Col 1, lines 36-43). In addition, Murata discloses that prior art switchers input and output lines are arranged in the form of a matrix so that it is possible to switch the output destinations of the input signals or simultaneously distribute the input signals to a plurality of output lines in accordance with a user's instruction (Col 1, lines 16-21).

Allowable Subject Matter

7. Claims 26,30-33,35-37,39,40,42 and 43 are allowed.

8. The drawings amendments were received on 3/18/04. These drawing corrections are approved.

Response to Arguments

Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Horabik can be reached on 703-305-4704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian A Zimmerman
Primary Examiner
Art Unit 2635

BAZ